PRODUCT BRIEF
June 2010

PROCe IV™

PCIe x4 Computation Accelerator

Key Features

- Stratix IV E 360, 530 and 820 FPGAs
- 4-lane PCI Express (PCIe x4) host interface
- Five level memory structure (**8.5 GB**+).
  Maximum sustain throughput of **4,693 GB/s** for internal memories and **12 GB/s** for DRAMs as follows:
  - Up to 1280 M9K (9K-bit) DPRAM blocks
  - Up to 64 M144K (144K-bit) RAM blocks
  - Up to 10,624 MLAB (320-bit) RAM blocks
  - A 512 MB DDR2 memory with **3.6GB/s** sustain throughput using up to 8 ports. (Up to 16 ports with lower access rate)
  - 2 DDR2 SODIMMs with up to **3.6 GB** each at a maximum sustain throughput of **7.2 GB/s**
- Supports 2 PROCe IV Type 1 Daughter Boards: Camera Links, SDI, User's Ethernet and other interfaces
- Typical system frequencies: 100-300 MHz
- Flexible clocking system
- Volatile and non-volatile design security
- Supported by GiDEL's ***PROC Developer's Kit***

Benefits

- Leading edge performance
- Advance development tools
- Low power consumption
- Maintainability
- Reliability
- Long life cycle

（写真のSDI 子ボード, SO-DIMMはオプションです）

Overview

The ***PROCe IV***™ system provides a high-capacity, high-speed FPGA-based platform fortified with high throughput and massive memory, resulting in a powerful and highly flexible system. The ***PROCe IV*** can be hosted via 4-lane PCI Express. The board's high speed performance coupled with memory and add-on daughter boards' flexible architecture enable the system to meet almost any computational needs. In addition to 512MB on-board memory, two SODIMM sockets provide up to 8GB of memory or additional connectivity and logic. Abundant memory conjoined with fast PCIe connection enable strong co-processing between a standard PC operating system and the FPGA acceleration. The ***PROCe IV*** system, with GiDEL's ***PROCDeveloper's Kit*** and tools, offers incredible performance yet supports quick implementation of your unique design. These unique features are achieved by eliminating the need for a high-speed board design, a PCI Express application driver, board constraints and environment FPGA code. The generated HDL code enables high throughput, easy-to-use parallel access to large memories. As a result, designers can focus on their proprietary value-added design. User designs may be in HDL, C-based, Simulink (graphical design) or any combination of them.

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Target Applications

- COTS acquisition and accelerator boards in:
  - ✓ HPC (High Performance Computing)
  - ✓ Machine Vision and Imaging
  - ✓ High performance acquisition systems
  - ✓ Bioinformatics Applications
- Small ASIC and SoC Prototyping
- Complex algorithm and IPs validation.

Development Environment

The ***PROCDeveloper's Kit***, GiDEL's intuitive design and debug environment, facilitates design development effort on the ***PROCe IV*** system. The kit contains ***PROCWizard***™, ***PROCMultiPort***™ and other memory control IPs, ***Quartus*** , ***USBBlaster***, and a ***PROC_HILs***™ option.

The ***PROCWizard*** performs hardware initialization and automatically generates the following:

- Interface documentation in HTML or Microsoft Word.
- C++ class(es) application driver(s) enable simultaneous accesses of multiple applications, each to its' dedicated section of the PROC board.

  Top-level designs, interface modules/entities and on-board memory controllers for application use.
- Device constraints (as pin-outs).

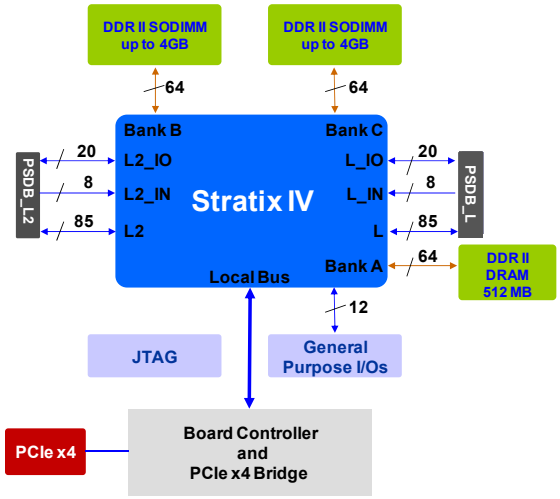
The ***PROCMultiPort*** and other memory control IPs provides simple access as FIFOs and frame delays to the on-board DRAM. It enables parallel access to the on-board memory while enabling to split the physical memory into multiple logical memories. As a result the main benefits are:

- Simplifies design and enhances system performance.
- Replaces the need for inventory of special memories by using standard memory and IP.

The ***USBBlaster*** enables visibility of internal signals using the available FPGA memory.

The ***PROC_HILs***™ enables the users to design in ***Simulink***™ while accelerating enormously the design simulation on the ***PROCe IV*** board. Alternatively, the ***PROC_HILs*** may be to used, via Simulink, as a design entry tool for an FPGA based accelerator.

Other high-level design entry options, such as C++, are available via GiDEL's partners.



PROCe IV Board

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